REMARKS

The Office Action dated August 7, 2003 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. Claims 8, 10, 13, and 14 are pending. In view of these remarks, Applicants request the favorable consideration of claims 8, 10, 13 and 14.

The Office Action rejected claims 8, 10, 13, 14 under 35 U.S.C. §103(a) as being unpatentable over Maesako et al. (U.S. Patent No. 6,016,280) in view of Rose et al. (U.S. Patent No. 5,471,421). The Office Action takes the position that the combination of Maesako and Rose teach or suggest all the features recited in claims 8, 10, 13 and 14. Applicants respectfully disagree.

Claim 8 is directed to a semiconductor memory device comprising a SRAM memory block provided on a chip. The SRAM memory block includes a first power pad and a SRAM cell array connected to the first power pad. A DRAM memory block is also provided on the chip. The DRAM memory block includes a second power pad and a DRAM cell array connected to the second power pad. A control unit controls the on/off of a source voltage supplied to the DRAM memory block via the second power pad, depending on whether the DRAM cell array is used to retain data, so that the source voltage supplied to the DRAM memory block is cut off when the DRAM cell array is not used.

Claim 13 recites a semiconductor memory device comprising a SRAM memory block provided on a chip, the SRAM memory block includes an SRAM cell array. A DRAM memory block is also provided on the chip. The DRAM memory block has a DRAM cell array. A control unit is connected to each of the SRAM memory block and the DRAM memory block. The control unit includes a first pad and a second pad. The control unit activates an operation of one of the SRAM memory block or the DRAM memory block based on a combination of a control value indicated by a first control signal presented to the first pad and a second control value indicated by a second control signal presented to the second pad. The control unit activates or deactivates operation of the DRAM memory block via the first and second pads, depending on whether the DRAM cell array is used to retain data, so that the operation of the DRAM memory block is deactivated when the DRAM cell array is not used.

Maesako is directed to a semiconductor memory device that includes a power

source voltage converter circuit which generates a first internal power source voltage and second internal power source voltage on the basis on an external power source voltage.

Maesako, however, does not teach or suggest a control unit controlling ON/OFF of a source voltage supplied to the DRAM memory block via the second power pad, depending on whether the DRAM cell array is used to retain data, so that the source voltage supplied to the DRAM memory block is cut off when the DRAM cell array is not used, as admitted by the Office Action. The Office Action utilizes Rose to teach this feature, however Applicants respectfully disagree with the Examiner's assertion that Rose cures the deficiencies of Maesako.

Ross is directed to a storage cell that includes a first bit line, a storage circuit, and a pass transistor. The DRAM storage cell 10 includes a pass N-MOSFET 12 having its drain coupled to a bit line BL and its source coupled to a storage node 14. A word line 16 is also provided to drive the word line WL of the DRAM 10. The word line driver 16 is coupled to the power supply VDD and to a power supply VSS1. The purpose of the word line driver 16 is to receive at its input WLORB a logic signal from a decoder circuit indicating that the DRAM storage cell 10 is to be accessed. When the storage cell 10 is accessed, the word line driver 16 drives the word line WL to VDD, thereby turning on the pass transistor 12.

However, the combination of Maesako and Rose fail to teach or suggest a control unit controlling ON/OFF of a source voltage supplied to the DRAM memory block via the second power pad, depending on whether the DRAM cell array is used to retain data, so that the source voltage supplied to the DRAM memory block is cut off when the DRAM cell array is not used. Rose merely discloses that the word line driver 16 which controls the on/off of a pass-transistor 21 by changing the gate level or the word line potential of the pass-transistor 12 to VDD or VSS1, depending on whether the DRAM cell is accessed or not. In other words, Rose does not teach or suggest controlling the source voltage that is supplied to a DRAM memory block via a power pad as in the claimed invention.

In addition, Figure 3 of Rose discloses the control circuit 16 being a level shifter, which shifts the input signal WLORB with a VDD-VSS amplitude to the output signal having the VDD-VSS1 amplitude. As a result, the invention of Rose reduces the leak current from the pass-transistor 12 (Fig. 1) by pulling the deactivation level of the word line WL below the ground level VSS down to VSS1. In other words, Rose discloses that the reduction of

the power consumption of the memory device can be achieved by the decrease of the deactivation level of the word line.

In contrast, the objective of the claimed invention is to reduce the power consumption of the semiconductor memory device containing DRAM and SRAM, when the DRAM is not used to retain data. According to the claimed invention, reduction of the power consumption of the memory device is achieved by the use of a control unit controlling the ON/OFF of a source voltage supplied to the entire DRAM memory block via the second power pad, depending on whether the DRAM cell array is used to retain data. Rose, however, does not teach or suggest controlling the supply of a source voltage to the entire DRAM memory block when it is not used to retain data, in order to reduce the power consumption of the memory device in which the DRAM and the SRAM coexist. Accordingly, Rose does not cure the deficiencies of Maesako. Thus, the combination of Maesako and Rose fail to teach or suggest a control unit controlling the ON/Off of a source voltage supplied to the DRAM memory block via the second power pad, depending on whether the DRAM cell array is used to retain data, so that the source voltage supplied to the entire DRAM memory block in response to a control signal which is externally supplied to the control unit. Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 8 and 13.

Claims 10 and 14 are dependent upon claims 8 and 13. It is respectfully submitted that claims 10 and 13 also recite subject matter that is patentable for at least the reasons mentioned above. Therefore, Applicants request the withdrawal of the rejection of claims 10 and 14 under 35 U.S.C. 103(a).

In view of the above remarks, Applicants request the withdrawal of the rejections to claims 8, 10, 13, and 14. It is respectfully submitted that the combination of Rose and Maesako fail to teach or suggest all the features of the claimed invention. Therefore, Applicants submit that the application is now in condition for allowance with claims 8, 10 and 13-14 contained therein.

Should the Examiner believe the application is not in condition for allowance, the Examiner is invited to contact Applicants' undersigned attorney at the telephone number listed below.

In the event this paper is not considered to be timely filed, Applicants respectfully

petition for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to Counsel's Deposit Account 01-2300.

Respectfully submitted,

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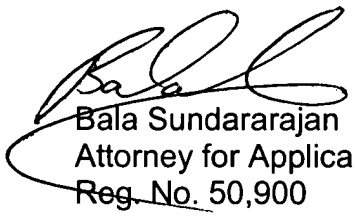

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